Remarks/Arguments

In the September 9, 2007 Office Action, the Examiner rejects Claims 5-7, 9-22 and 24-26 under 35 USC § 103(a). To better clarify the invention, Applicant has amended Claims 5-7, 11, 13-16, 18-22, 24-26; canceled Claims 8-10, 12, and 17; and added new Claims 29-40. Support for the amendments and the new claims is provided throughout the specification. Claims 5-7, 11, 13-16, 18-22, 24-26 and 29-40 are now pending. Applicant respectfully requests reconsideration of the patentability of the claims of the present application in view of the following remarks.

Rejection Under 35 USC § 103(a)

Claims 5-7:

The Examiner rejects Claims 5-7 under 35 USC § 103(a) over Yang (US Patent No. 6,526,446) in view of Savarda (US Pub. No. 2003/0196081). Applicant overcomes the rejection as follows.

Neither Yang nor Savarda, in combination or by themselves disclose all the elements of amended Claim 5. In particular, Yang and Savarda do not disclose "a hardware engine for completely offloading Transmission Control Protocol/Internet Protocol (TCP/IP) protocol processing both in a transmit path and a receive path from a host system software stack, comprising: an inbound MAC Receive state machine for receiving a network packet and passing the network packet to an inbound memory buffer; an inbound IP verifier hardware state machine for verifying IP packet headers if the received packet from the network is an IP packet; an inbound IP fragment processing state machine for processing and reassembling IP packet fragments into an IP datagram that is stored in a local memory for the hardware engine; wherein the inbound IP fragment processing state machine assigns a timer to each IP datagram with a timeout value, and if a timeout occurs then the entire datagram is removed from a reassembly list and storage space associated with the timed out datagram is assigned to a free buffer list that is maintained by a buffer list manager, where the buffer list manager implements a hardware state machine to manage storage space in the local memory and

grants free buffer space when available to the inbound IP verifier hardware state machine ; and an inbound TCP hardware state machine for (a) processing TCP segments received from an IP layer by completely offloading TCP/IP protocol stack processing from the host system software stack to hardware; (b) re-ordering out of order TCP segments and then transferring the TCP data to the host system; and (c) transferring data from an iSCSI connection to a processor that processes iSCSI frames; wherein the inbound TCP hardware state machine retrieves a network control block from a TCP table manager and updates network state information in the network control block and maintains a segment reassembly list for each network connection; wherein the inbound IP verifier state machine passes non-IP data packets to the host system via an inbound direct memory access engine (IDE). (Amended Claim 5).

Yang only discloses a TCP segmentation functionality for transmitting data from a host memory to a network, unlike the hardware engine of amended Claim 5 that completely offloads TCP/IP protocol processing from a host system software stack for network traffic sent to the network or received from the network. On Page 3, Section 7 of the office action, the Examiner cites various sections of Yang to reject certain elements of previously presented Claim 5. Applicant addresses those references below:

(a) Col. 2, line 35-37 for rejecting the "inbound MAC receive state machine": Yang in this segment deals with a circuit that receives data from the host system and then segments the TCP data. Yang does not disclose in this section an "input" path (i.e. data received from the network and sent to the hosts) and hence fails to disclose the inbound MAC receive state machine.

(b) Col. 9, lines 21-32 for rejecting the "inbound IP verifier state machine": Yang in this segment mentions a checksum circuit 216 used for error detection on data that is transmitted by NIC 120. Once again, this is the transmit path and does not address what happens to TCP/IP offload when data is received by NIC 120, rather than being transmitted by NIC 120.

(c) Col. 9, lines 11-20 for rejecting the "inbound IP fragment processing state machine": Yang in this segment mentions an alignment circuit 215 that aligns data that is transmitted by NIC 118. As discussed above, the claimed inbound

IP fragment processing state machine deals with traffic received from the network and hence is not disclosed by Yang.

(d) Col. 6, lines 51-55 for rejecting the "inbound TCP state machine": Yang in this segment describes a TCP segmentation state machine 208 that segments data into Ethernet frames. Once again, this deals with outgoing traffic from NIC 118 and does not involve incoming traffic.

Applicant has reviewed the Yang reference in detail and believe that the amended Claim 5 elements are not disclosed anywhere in Yang.

The Examiner acknowledges and Applicant agrees that Yang fails to disclose that "inbound IP verifier state machine passes non-IP data packets to a host". One reason why Yang does not disclose this feature is because Yang does not show an offload, hardware engine as claimed in amended Claim 5 for processing received network packets.

The Examiner relies on Savarda, (Paragraph [0029]) to reject the foregoing element (i.e. inbound IP verifier state machine passes non-IP data packets to a host). Applicant respectfully disagrees with the reliance on Savarda because Savarda fails to cure the deficiencies of Yang.

Savarda discloses a packet co-processor for implementing the IPSec protocol (See Savarda, Paragraph [0024]) and does not disclose a hardware engine as articulated by amended Claim 5. Paragraph [0029] simply describes creating a packet object header to process a packet, as an IP packet or as a non-IP packet and does not disclose any of the elements of amended Claim 5.

Support for the Claim 5 amendments is provided in the referenced paragraphs. The underlined sections show the claim additions:

(a) an inbound MAC Receive state machine for receiving a network packet and passing the network packet to an inbound memory buffer; **[Paragraph 102]**

(b) an inbound IP verifier hardware state machine for verifying IP packet headers if the received packet from the network is an IP packet; **[Paragraphs [0161]-[0164]]**

(c) an inbound IP fragment processing state machine for processing and reassembling IP packet fragments into an IP datagram that is stored in a local memory for the hardware engine; wherein the inbound IP fragment processing state machine assigns a timer to each IP datagram with a timeout value and if a timeout occurs then an entire datagram is removed

from a reassembly list and storage space associated with the timed out datagram is assigned to a free buffer list that is maintained by a buffer list manager, where the buffer list manager implements a hardware state machine to manage storage space in the local memory and grants free buffer space when available to the inbound IP verifier hardware state machine; **[Paragraphs [0166] –[0169]];** and

(d) an inbound TCP hardware state machine for (a) processing TCP segments received from an IP layer by completely offloading TCP/IP protocol stack processing from the host system software stack to hardware; (b) re-ordering out of order TCP segments and then transferring the TCP data to the host system; and (c) transferring data from an iSCSI connection to a processor that processes iSCSI frames; wherein the inbound TCP hardware state machine retrieves a network control block from a TCP table manager and updates network state information in the network control block and maintains a segment reassembly list for each network connection; [**Paragraphs [0172] to [175]**]

Claims 6 and 7 depend from Claim 5 and are patentable over Yang and Savarda based on at least the reasons given above with respect to Claim 5.

Therefore, based on at least the foregoing reasons, Claims 5-7 are patentable over Yang and Savarda. Applicant respectfully request allowance of Claims 5-7.

Claims 9-10:

The Examiner rejected Claims 9-10 over Yang in view of Trippe (US 2003/0108066). Applicant has Canceled Claims 9-10 to expedite prosecution, without prejudice.

Claims 11-14, 16, 18 and 22:

Claims 11-14, 16 18 and 22 are rejected over Yang and Hayes (US 2003/0046330). The Examiner relies on Hayes to disclose "an auxiliary processor that can process TCP segments for iSCSI (See paragraph 0017)" (See Office Action, Page 5, Section 9). Applicant overcomes the rejection as described below.

Claim 11:

Hayes fails to cure the deficiencies of Yang, described above with respect to Claim 5. Hayes discloses "selective offloading of protocol processing" (See Hayes Abstract), because complex processing is still performed by the host processor. Independent Claim 11 discloses a complete offload of TCP/IP operations both for sending and receiving data. In contrast, Hayes in Paragraph [0025] describes the problems associated with a complete offload solution. The inventive embodiments solve this problem by providing the claimed system. If anything, Hayes teaches away from the elements of amended Claim 11. Paragraph 0017 of Hayes simply provides a generic description for offloading iSCSI operations.

Therefore, Hayes does not add anything to deficiencies of Yang and Claim 11 is patentable over Yang and Hayes.

Support for Claim 11 amendments is provided in the referenced paragraphs shown below:

a first in-bound transmission control protocol (TCP) processor for (a) processing TCP segments received from a network by completely offloading a TCP/IP (Internet Protocol) protocol stack processing from a host system software stack to hardware; (b) re-ordering out of order TCP segments and then transferring TCP data to the host system; and (c) transferring data from an iSCSI connection to a second in-bound processor that processes iSCSI frames and non-TCP data; wherein the first in-bound TCP processor retrieves network control blocks and updates network state information in the network control block and maintains a segment reassembly list for each network connection; [**Paragraphs [0172] to [175]**]

a first outbound processor that obtains connection state information from a network control block; builds a TCP header and sends TCP data to the network; [**Paragraphs [0135] to [138]**]

a second outbound processor that processes media access control (MAC) and IP transfer requests; [**Paragraphs [0141] to [147]**]

a fragment processor that receives data packet fragments and reassembles the data packet fragments into complete datagrams for delivery; wherein the fragment processor assigns a timer to each datagram with a timeout value and if a timeout occurs then an entire datagram is removed from a reassembly list and storage space associated with the timed out datagram is assigned to a free buffer list that is maintained by a buffer list manager, where the buffer list manager implements a hardware state machine to manage storage space in a local memory and grants free buffer space when available to the verification module; **[Paragraphs [0166] –[0169]];**

a third outbound processor for processing small computer system interface (SCSI) requests received from the host system via a hardware TCP stack; [**Paragraph 0200**] and

a TCP Table manager that interfaces with the first outbound TCP processor, the first in-bound TCP processor, the second in-bound processor and the third outbound processor; the TCP Table Manager maintains timer functions for all TCP connections at any given time in the hardware engine and maintains a linked list of network control blocks for processing network data sent by the hardware engine and received by the hardware engine. [**Paragraph [0182]-[0185]]**

Claims 13-14, 16, 18 and 22:

Claims 12 is Canceled and Claims 13-14, 16, 18 and 22 depend from Claim 11 and hence are patentable over Yang and Hayes for the reasons given above with respect to Claim 11. Applicant respectfully requests allowance of Claim 13-14, 16, 18 and 22.

Claim 15:

The Examiner rejected Claim 15 under 35 USC § 103(a) in view of Yang, Hayes and Savarda. Claim 15 depends from Claim 11 and is patentable over Yang, Hayes and Savarda for at least the same reasons given above with respect to Claim 11. Applicant respectfully requests allowance of Claim 15.

Claim 17:

The Examiner rejected Claim 15 under 35 USC § 103(a) in view of Yang, Hayes and Chang (US Patent No. 7,103,317). Claim 17 depends from Claim 11 and is patentable over Yang, Hayes and Chang for at least the same reasons given above with respect to Claim 11. Chang fails to cure the deficiencies of Yang and Hayes. Applicant respectfully requests allowance of Claim 15.

Claim 19 and 20:

The Examiner rejected Claims 19 and 20 under 35 USC § 103(a) in view of Yang, Hayes and Trippe. Claims 19 and 20 depend from Claim 11 and are patentable over Yang, Hayes and Trippe for at least the same reasons given above with respect to Claim 11 because Trippe does not cure the deficiencies of Yang and Hayes. Applicant respectfully requests allowance of Claims 19 and 20.

Claim 21:

The Examiner rejected Claim 21 under 35 USC § 103(a) in view of Yang, Hayes and Boucher (US Patent No. 6,247,060). Claim 21 depends from Claim 11 and is patentable over Yang, Hayes and Boucher at least for the reasons given above with respect to Claim 11 because Boucher does not cure the deficiencies of Yang and Hayes. Applicant respectfully requests allowance of Claim 21.

Claims 24 and 26:

The Examiner rejected Claims 24 and 26 under 35 USC § 103(a) in view of Yang, and Boucher (US Patent No. 6,247,060).

Support for Claim 24 and 26 amendments are provided in **Paragraphs [0366] to [0373] and [0388] to [0390]**.

Claims 24 and 26 are patentable over Yang and Boucher at least for the reasons given above with respect to Claim 11 because Boucher does not cure the deficiencies of Yang. Applicant respectfully requests allowance of Claims 24 and 26.

New Claims 29-40:

New Claims 29-40 are patentable over the cited art for at least the reasons given above. Applicant respectfully requests allowance of new claims 29-40.

Conclusion

For the foregoing reasons, Applicant believes Claims 5-7, 11, 13-16, 18-22, 24-26 and 29-40 are allowable, and a notice of allowance is respectfully requested. If the Examiner has any questions regarding the application, the Examiner is invited to call the undersigned at (949)-955-1920.

Respectfully submitted,

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